- Performing selection and permutation on said memories, and
- Reading out said data entities in said permuted memories, in a memory-by-memory fashion.

2. (Amended) Method as in claim 1, wherein said data entities are logical ones and zeros.

3. (Amended) Method as in claim 1, wherein said data entities are multiple bit words.

4. (Amended) Method as in claim 1, wherein said data entities are three bit words.

5. (Amended) Method as in claim 1, wherein the number of columns used in the column interleaver function is changed on the fly, said number of columns not exceeding said maximum number of columns.

6. (Amended) A module for column interleaving, comprising means for applying a method to implement a column interleaving function, comprising the steps of:

- Providing a number of memories equal to the maximum number of columns in the interleaver function,
- Inputting a stream of data entities,
- Writing said data entities successively into a memory, until all memories are completely filled or until all data entities are written,
- Performing selection and permutation on said memories, and
- Reading out said data entities in said permuted memories, in a memory-by-memory fashion.

7. (Amended) An integrated circuit device, comprising a module for column interleaving, comprising means for applying a method to implement a column interleaving function, comprising the steps of:

- Providing a number of memories equal to the maximum number of columns in the interleaver function,
- Inputting a stream of data entities,
- Writing said data entities successively into a memory, until all memories are completely filled or until all data entities are written,

  Performing selection and permutation on said memories, and